ABSTRACT

An apparatus and method for monitoring memory system performance and controlling an operating parameter is provided. A plurality of digital events indicative of memory system operations is detected, from which a subset of digital events to count is periodically selected, the subset being those digital events occurring during a sampling window time interval. Responsive to each digital event of the subset, a transistor is switched on to conduct current from a power supply to a capacitor. The transistor is biased by the capacitor to operate in a constant current region providing a substantially fixed amount of charge added to the capacitor responsive to each digital event of the subset. The operating parameter is controlled responsive to the charge accumulated in the capacitor, representative of the count of digital events in the subset. In one embodiment, the sampling window time interval is selected pseudo-randomly within a periodic base time interval.